DISK SYNCHRONOUS WRITE

CROSS-REFERENCE TO RELATED APPLICATIONS

[01] This application claims the benefit of Provisional Application No. 60/451,458, filed April 8, 2003. This application incorporates these provisional applications by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[02] This invention relates in general to the field of information storage, and more particularly to read/write channel control devices that can generate timing signals for controlling read/write operations in rotating magnetic storage devices.

2. Description of the Related Art

[03] Hard disk drives (HDD) typically comprise at least one disk having a magnetic medium for storing information, a spindle, a controller for controlling disk rotational speed, a read/write head and actuator assembly for positioning the head over the appropriate disk track, and data channels for reading data from the disk and writing data to the disk. The read/write head reads data from and writes data to the disk in data blocks having either fixed or variable length. A data block comprises a preamble (for acquiring timing signals), timing bits, address bits, data bits, and error correction bits. Data blocks are recorded in sectors in concentric tracks and a track may comprise several sectors. The number of sectors may depend on the radial location of the track on the disk.

[04] In efforts to increase data density, HDD manufacturers write data to disks such that data density is substantially uniform throughout the disk. Uniform density requires a write clock that is synchronized to disk speed (disk speed being defined as the speed of the disk media relative to a specific point such as a write head). There are three sources of variation in disk speed: uncertainty of rotational speed, eccentricities of the disk to the spindle caused by disk slip, and location of data sectors relative to the axis of rotation.

[05] Rotational speed is uncertain because spindle speed control is not perfect in disk drives. Most HDDs have spindle speed specifications of +/- 0.1% absolute variation. Because uncertainty in the spindle speed results in a lower format target, engineers design

margins to allow the HDD to continue functioning under the worst-case spindle speed variation. For example, a sector written at a fixed +0.1% higher spindle speed and read at -0.1% lower spindle speed will experience a read data-rate 0.2% lower than the nominal read speed. In order for the read timing loop to lock properly to this lower data rate, the data sector requires a longer preamble, resulting in lower format efficiency. Also, in order to prevent writing over part of the preceding or the succeeding sector that was previously written at a different spindle speed, a larger gap between sectors must be allocated to provide a buffer zone. This larger gap also reduces the overall format efficiency of the drive.

[06] In addition to the longer preamble required to enable timing loop lock to a read-back waveform, it is also often necessary to increase the timing loop bandwidth, resulting in a higher read error rate. Read error rate is lower when the read timing loop bandwidth is lower.

[07] Disk slip is due to manufacturing tolerances creating eccentricities between the disks and the spindle mechanism. When HDDs experience a large lateral shock, the disk may slip relative to the spindle, causing the tracks to be placed on circular paths off-center from the axis of rotation. When reading or writing data, this off-center rotation appears to be a variation of spindle speed. Data read from a sector written prior to a disk slip will have an even larger frequency offset than the nominal value.

[08] Disk slip has sinusoidal sector-to-sector timing variation. The variation in the time interval between sectors appears as a spindle speed variation even though the variation may be due partially to disk slip. Although this component of variation is repeatable around the disk, data written to a disk before the disk slip may be read after the disk slip, resulting in an unpredictable disk read. In many HDDs, a disk slip creates a read frequency offset as large as 0.5% of nominal, which is larger than normal spindle speed variation.

[09] Some modern read channels employ digital timing recovery loops and already have a capability to adjust the read back initial frequency offset if the offset amount is known. Fig. 1 shows an example of a phase-locked loop (PLL) circuit for adjusting the frequency of the read channel to compensate for a known frequency offset. The phase detector 102, low pass filter 103, voltage controlled oscillator (VCO) 104, and divider 105 are part of a PLL time base generator 101. The read clock interpolator 106, normally used for read clock timing, is

outside the time base generator loop and is responsive to a known frequency offset signal 108 to provide a modified frequency output signal 109.

[10] Disk speed variation is also due to the location of data sectors relative to the axis of rotation. As a data sector is written farther from the center of the disk, the physical length of the sector increases unless the write clock frequency also increases. Timing circuits also may use one or more interpolators to pre-compensate the write clock to change the write density according to the track location on the disk. Fig. 2 shows that a clock interpolator 206 may also be used to provide pre-compensation for adjusting the data write density necessary to compensate for the track location on the disk. The write pre-compensation control signal 208 adjusts the clock interpolator 206 to account for track location on the disk, thereby providing a pre-compensated clock signal 209. However, if the interpolator has to perform frequency adjustments in addition to pre-compensation adjustments, then the design of the control logic and clock interpolators becomes significantly more complicated.

[11] Therefore, a need exists for circuitry that adjusts the write clock frequency in response to apparent disk speed variations and pre-compensation controls.

SUMMARY OF THE INVENTION

[12] To address the stated need and fulfill other desired objectives, in accordance with one embodiment of the invention, a time base generator provides a clock signal to a clock interpolator responsive to a phase rotation control signal. The phase rotation interpolator adjusts the time base generator output to provide a modified clock signal that is synchronous with the apparent disk speed. A timing apparatus generates the phase rotation control signal, wherein the phase rotation control signal is dependent upon the period between adjacent sector sync-marks. For example, if the period between adjacent sector sync-marks is increased by 0.1 percent, the modified clock signal must be increased by 0.1 percent to provide a constant bit density. This embodiment is most useful when pre-compensation control is provided separately.

[13] In another embodiment, a time base generator provides a clock signal that is already modified to the desired frequency before sending it to the pre-compensation block. In accordance with one embodiment of the invention, a timing circuit incorporates a phase

rotation control clock interpolator in the feedback path of the time base generator. The pre-compensation control interpolator is outside the feedback loop. Within the feedback loop, the phase rotation control interpolator increases the VCO output frequency by slowing its own output.

[14] An additional benefit of placing the phase rotation control interpolator in the feedback loop is that the clock output from the VCO is cleaner than the clock output of the interpolator. Interpolators generally have 6 to 7 bit precision and the resulting timing signal has phase noise at the output of the interpolator. By placing the phase rotation control interpolator inside the feedback loop, the output of the phase rotation control interpolator is significantly filtered by time base generator loop filter.

[15] In yet another embodiment, the invention incorporates a mode control for selecting between a read and a write mode. In the read mode, the invention provides a modified frequency clock for acquiring a preamble, wherein the clock is adjusted for the apparent disk speed. In the write mode, the invention provides a clock output that incorporates both an adjustment for the apparent disk speed and pre-compensation control.

BRIEF DESCRIPTION OF THE DRAWINGS

[16] Figure 1 shows a block diagram of a conventional circuit for adjusting a read channel timing frequency based upon frequency offset control.

[17] Figure 2 shows a block diagram of a conventional circuit for adjusting a write channel timing frequency based upon fixed pre-compensation timing values.

[18] Figure 3 depicts one embodiment of the invention, wherein a clock interpolator is used to adjust the output frequency responsive to phase rotation.

[19] Figure 4 depicts another embodiment of the invention, wherein one interpolator for adjusting the frequency relative to phase rotation is placed within the feedback loop of a phase-locked loop, and a second interpolator responsive to pre-compensation control is placed outside the feedback loop.

[20] Figure 5 depicts yet another embodiment of the invention, wherein the circuit may be configured for either writing data to a disk or reading data from a disk.

[21] Figure 6 shows the configuration of the mode control for the write mode.

[22] Figure 7 shows the configuration of the mode control for the read mode.

[23] Figure 8 is a schematic representation a hard disk drive system showing the major components.

[24] Figure 9 depicts still another embodiment of the invention, wherein the circuit may be configured for either writing data to a disk or reading data from a disk.

DETAILED DESCRIPTION OF EMBODIMENTS

[25] The inventive apparatus controls the write frequency so that it is proportional to the sector-to-sector timing. Therefore, the actual data bit spacing on the disk and the physical size of the sector will be a substantially constant value regardless of the apparent disk speed variation caused by either normal spindle speed variation or disk slip.

[26] As shown in Fig. 8, a hard disk drive system comprises a disk having magnetic media 806. The motor 807 spins the disk at a constant speed and under control of the motor controller 808. While a constant speed is desirable, the speed varies within a certain tolerance. Data 810 passes through a read/write channel 803 to a recording head 805. The actuator 804 positions the recording head 805 over the proper data track, and data is transmitted to or from the read/write channel 803. A clock 801 responsive to a reference frequency 809 provides timing signals to the read/write channel 803, and the sector timing controller 802 synchronizes the clock 801 with the disk rotation. Fig. 8 is intended to be schematic of a hard disk drive, and skilled practitioners in the art will recognize that other configurations are possible.

[27] Initially, a timing circuit measures the time difference between consecutive sector sync-marks. Assuming that the actual spatial distances between sector sync-marks are nearly constant, any change from this number will indicate a need to modify the write speed clock to obtain constant write bit density. For example, if the timing between two consecutive sector sync-marks is increased by 0.1%, the write clock period must also be increased by 0.1% to obtained a fixed write bit size. If any sector sync-mark cannot be found, the timing difference between the missing sync-mark and the two neighboring sync-marks cannot be computed. The last available sector sync-mark timing value then may be used because speed

variations usually change slowly. Alternatively, an average of sector sync-mark timing values may be used to supply a missing sector sync-mark measurement.

[28] Sector-to-sector sync mark timing may also be used to set the read frequency offset value. An increased spacing between the sector sync marks will also increase the read-back sampling clock period, resulting in a small difference between the initial read-back waveform and the sampling clock. Because of this small difference, the read-back clock operates with a smaller bandwidth.

[29] Regular phase-locked loop (PLL) time base generators (frequency synthesizers) with M dividers have not provided sufficient frequency resolution to enable writing data at a synchronous frequency. High quality fractional synthesizers do not have sufficient bandwidth and thus may not be fast enough to change frequency quickly. A clock interpolator is already available in a read channel and takes a clock from a time base generator to generate a different frequency clock output very quickly and with very high resolution.

[30] A first embodiment of the invention is shown in Fig. 3. As in Figs. 1 and 2, PLL time base generator 301 comprises a phase detector 302 coupled to a low pass filter 303 providing a signal to a voltage controlled oscillator (VCO) 304. The output of the VCO 304 is passed through an M-divider circuit 305 and provides feedback to the phase detector 302. The output of the phase detector is a voltage proportional to the difference of the reference frequency 307 and the output of the M-divider circuit 305. After passing through the low pass filter 303, the phase detector voltage is the input voltage to the VCO 304, wherein the VCO 304 provides an output frequency proportional to the input voltage. The PLL is "locked" when there is a constant difference, usually zero, between the reference frequency 306 and the feedback signal (the output of the M-divider 305).

[31] The clock interpolator 306 modifies the PLL frequency proportional to the phase rotation control signal 306. As is known in the art, an interpolator circuit can shift the phase of a clock signal by small amounts in response to an external signal. In this case, the sector-to-sector timing signal provides the phase rotation control signal 308 to adjust the time base generator 301 output, thereby achieving the modified frequency clock output 309.

[32] In the present embodiment, if the spacing between two consecutive sector timing marks is increased by 0.1 percent, then the period of the modified frequency clock 309 is increased by 0.1 percent. In this manner, data bits written to the magnetic media occupy a substantially fixed amount of space regardless of the apparent disk speed variation. This embodiment may also be used to generate a read clock for read timing acquisition.

[33] This embodiment is useful for systems having a separate pre-compensation control. Combining the phase rotation control and pre-compensation control raises the complexity of controlling the interpolator.

[34] To avoid this additional complication, another embodiment of the invention provides for phase rotation control in the feedback loop and pre-compensation control outside the feedback loop, as shown in Fig. 4. The output of the VCO 404 provides input to both the pre-compensation clock interpolator 406 and the phase rotation clock interpolator 410. The pre-compensation control 408 controls the pre-compensation clock interpolator 406, and the phase rotation control 411 controls the phase rotation clock interpolator 410. The phase rotation clock interpolator 410 and the M-divider 405 are in the feedback loop of the PLL time base generator 401. In this embodiment, the phase rotation clock interpolator 410 controls the VCO 404 inversely. For example, the phase rotation clock interpolator 410 slows to increase the VCO 404 frequency.

[35] One additional benefit of placing the phase rotation interpolator 410 in the feedback path is that the clock output from VCO 404 generally is cleaner than the clock output of an interpolator. Interpolators typically have 6 to 7 bit precision, resulting in phase noise at the output of the interpolator. By placing the phase rotation interpolator 410 inside the feedback loop of the time base generator 401, the low pass filter 403 significantly filters the output of the interpolator 410, thereby providing a cleaner clock signal.

[36] Another embodiment, shown in Fig. 5, provides an adjusted clock frequency that may be used in both the read mode and the write mode. The mode control 513 determines whether the circuits are in a read or a write mode. In the write mode, the circuit operates as shown in Fig. 4. In the read mode, the PLL time base generator 501 receives feedback directly from the VCO 504, and the phase control clock interpolator 510 is configured to be

outside the feedback loop to provide the frequency modulated clock signal 512. In the read mode, the phase rotation interpolator is responsive to a frequency offset signal.

[37] In the write mode, the mode control configures the circuits to incorporate the phase rotation clock interpolator 510 in the PLL time base generator 501 feedback loop, and further configures the VCO 504 to provide a signal to the pre-compensation clock interpolator 506. The pre-compensation clock interpolator then provides the pre-compensated clock signal 509 responsive to the pre-compensation control 508.

[38] Figs. 6 and 7 schematically show how the control mode interconnects with other circuit elements for the write mode (Fig. 6) and the read mode (Fig. 7). Skilled artisans will recognize that implementation of the mode control must be done electronically rather than mechanically as shown.

[39] Yet another embodiment, shown in Fig. 9, includes a mode selector 911 for selecting between a read mode and a write mode, wherein the mode selector provides an enabling signal to each of the phase rotation clock interpolator 910 and the pre-compensation clock interpolator 906. The mode selector determines whether the pre-compensated clock signal 909 is responsive to the phase rotation clock interpolator 910 only or both the phase rotation clock interpolator 910 and the pre-compensation clock interpolator 906. When the read mode is selected, the pre-compensation clock interpolator 906 is disabled and the phase rotation clock interpolator 910 is enabled, and the pre-compensated clock signal 909 is responsive only to the phase rotation clock interpolator 910. In the write mode, both interpolators are enabled and the pre-compensated clock signal 909 is responsive to both. When an interpolator is disabled, the interpolator passes the clock signal from the input to the output unmodified. When enabled, the interpolator adjusts the input clock frequency according to the reference, and provides a modified output signal.

[40] Therefore, the foregoing is illustrative only of the principles of the invention. Further, those skilled in the art will recognize that numerous modifications and changes are possible, the disclose of these embodiment does not limit the invention to the exact construction and operation, and accordingly, all suitable modifications and equivalents, fall within the scope of the invention.